WHAT IS CLAIMED IS:

1. A fault insertion system resident in an integrated circuit, said fault insertion system having a source for an external assert signal and a source for register values, said integrated circuit having a one or more circuit nodes receiving normal system signals, said fault insertion system comprising:

a Fault Apply Register (FAR) operated to receive FAR codes from said source for register values, said FAR codes having values associated with a fault-on code and a fault-off code;

a FAR decode block connected to said FAR and operated to decode said FAR codes and assert a FAR decode block output signal when said FAR contains said fault-on code, and to deassert said FAR decode block output signal when said FAR contains said fault-off code;

an External Control Bit (EXT) operated to receive EXT values from said source for register values, said EXT values associated with set or not set;

a first logic connected to said EXT and said external assert signal, and operated to assert a first logic output signal when said EXT contains said not set value or when said EXT contains said set value and said external assert signal is asserted;

a second logic connected to said FAR decode block output signal and said first logic output signal, and operated to assert a second logic output signal when said FAR decode block output signal is asserted and said first logic output signal is asserted;

a Fault Identification Register (FIR) operated to receive a FIR code from said source for register values, said FIR code being one of a set of FIR codes, each of said FIR codes having a value associated with a desired fault;

a FIR decode block connected to said FIR and said second logic output signal, and operated to decode said

FIR code and assert a FIR decode block output signal while said second logic output signal is asserted; and

a circuit node fault logic block connected to said FIR decode block output signal and one of said circuit nodes, and operated to apply said normal system signals to said circuit node when said FIR decode block output signal is not asserted, and to apply a test signal to said circuit node while said FIR decode block output signal is asserted.

2. A fault insertion system according to claim 1, wherein said FIR decode block output signal comprises a plurality of fault signals, and said fault insertion system further comprises a plurality of node fault logic blocks, each of said node fault logic blocks connected to one or more of said fault signals and one of said circuit nodes.

3. A fault insertion system according to claim 1, wherein said source for register values comprises a microprocessor.